Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50968

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is threshold voltage of MOS transistor?
2. Show how nMOSFET acts as a switch?
3. What is stick diagram? Draw the stick diagram for two input NAND gate.
4. Realize the two input NAND gate using pass transistor logic.
5. Differentiate latches and registers.
6. What is clock skew? How to overcome clock skew?
7. Find the propagation delay of n-bit carry select adder.
8. Write the logic equation for the 3-bit magnitude comparator.
9. List the issues in testing microchip design process.
10. What are the different types of ASICs?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Obtain the drain current in three different regions of operation. (7)

(ii) Show how channel length modulation affects the drain current and body effect affects the threshold voltage? (6)

Or

(b) What is the dynamic condition of MOSFET? Discuss the transistor characteristics of MOSFET under dynamic conditions. (13)

12. (a) (i) Find the Elmore's constant of the 4-input NAND gate. (7)

(ii) Realize the 4:2 encoder using CMOS logic. (6)

Or

(b) (i) Explain the concept of dynamic logic. Realize the 3-input NAND gate using dynamic logic. (7)

(ii) Describe the disadvantages of dynamic logic. Provide the solution to overcome the dynamic logic. (6)

13. (a) Elucidate the static latches and registers suitable for sequential logic circuit design. (13)

Or

(b) (i) Draw the monostable multivibrator using CMOS transistor and explain the operation. (7)

(ii) What are the timing classification of digital systems? Show how the timing is applied for synchronous design. (6)

14. (a) (i) What is the need for carry save adder? Explain the 4-bit carry save adder. (6)

(ii) What is an array multiplier? Show how array multiplier uses an array of cells for computing the result. (7)

Or

(b) Illustrate the hierarchical memory architecture and explain the building blocks of memory architecture. (13)

15. (a) (i) What are the faults in ASIC design? Model the faults in ASIC design. (7)

(ii) Explain the design flow process suitable for ASIC. (6)

Or

(b) (i) Write the test bench in Verilog HDL for a combinational circuit. (6)

(ii) Explain the test interface and boundary scan suitable for scan design. (7)

PART C — (1 × 15 = 15 marks)

16. (a) (i) What is pipelining? Apply the pipelining concept and find the total clock time required for obtaining outputs for $y = |a_n + b_n|$ where $n = 1, 2, 3, 4, 5$. (7)

(ii) Realize the function $F = \Sigma m(1, 5, 6, 7)$ using (8)

(1) Pseudo nMOS logic

(2) Static CMOS logic.

Or

(b) (i) Generate the test vectors for the combinational function $F = (AB + BC + CD)$ using automatic test pattern generation for the stuck-at-0 fault at node B. (8)

(ii) Realize the functions $F_1 = X_0 X_1 + X_1' X_2'$; $F_2 = X_0' X_1' + X_1 X_2$ sing programmable logic array. (7)